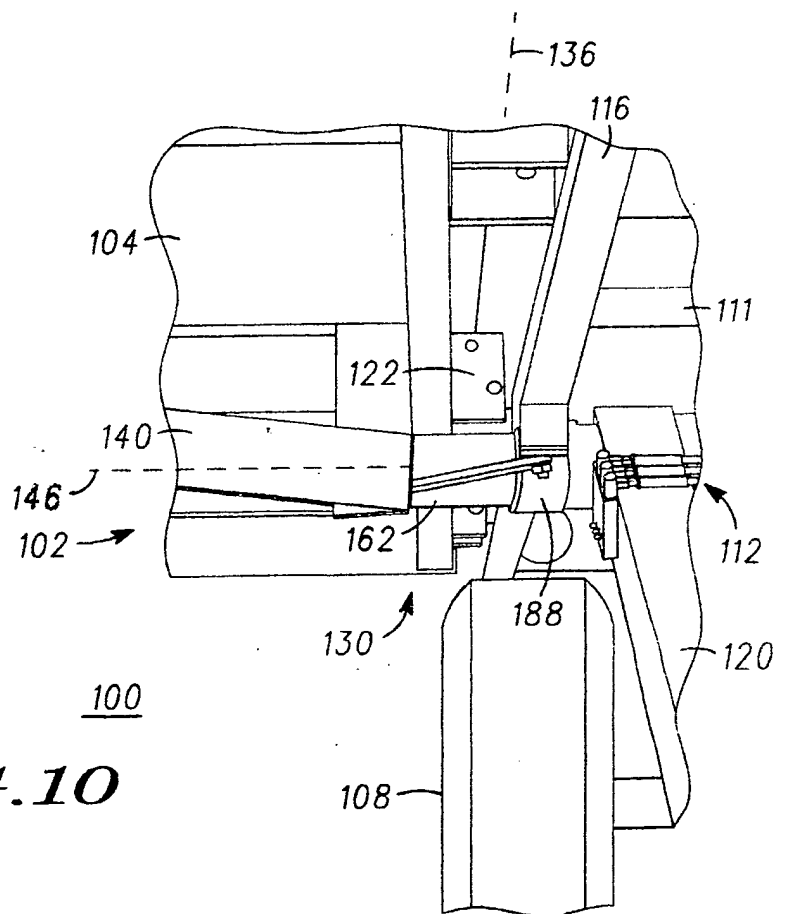
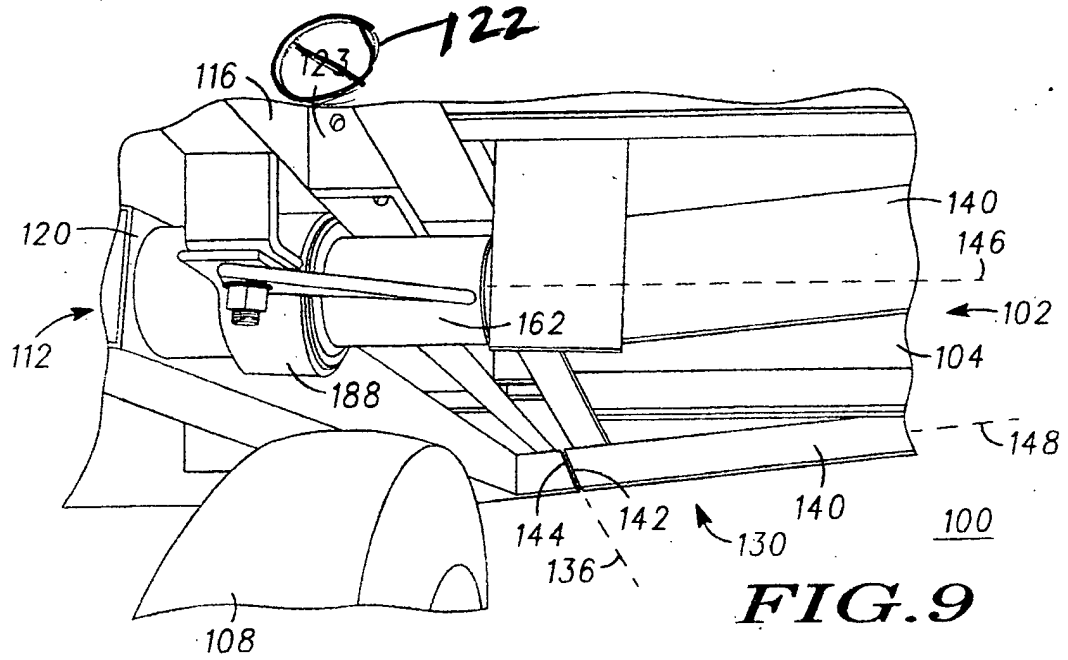


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A detailed cross-sectional view of a semiconductor device. A central vertical channel 104 is formed through a substrate 100. The channel is lined with a conductive material 125. Above the channel, a gate stack 105 is formed, consisting of a gate dielectric layer 122 and a gate electrode layer 124. The gate stack is connected to a horizontal bus bar 116 via a contact plug 122. The bus bar 116 is supported by a base layer 113. On either side of the channel, there are source/drain regions 108 and 112, which are separated from the channel by spacers 192. The entire device is covered by a protective layer 128. Various other layers and contacts are labeled with reference numerals.

[illegible]

FIG. 29

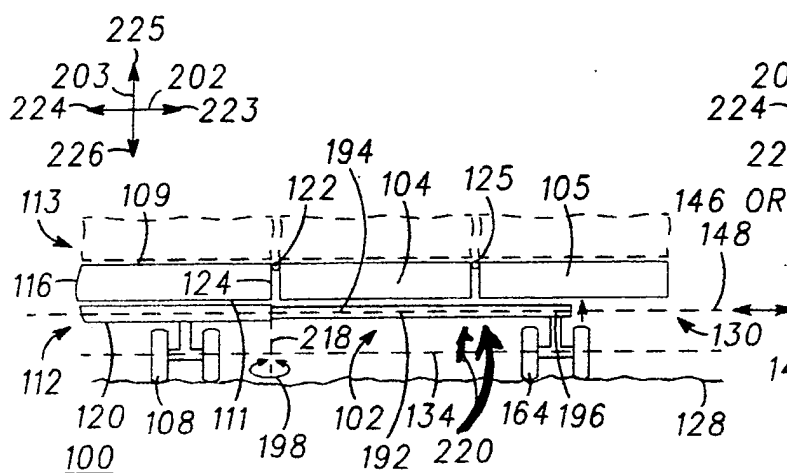


FIG. 30

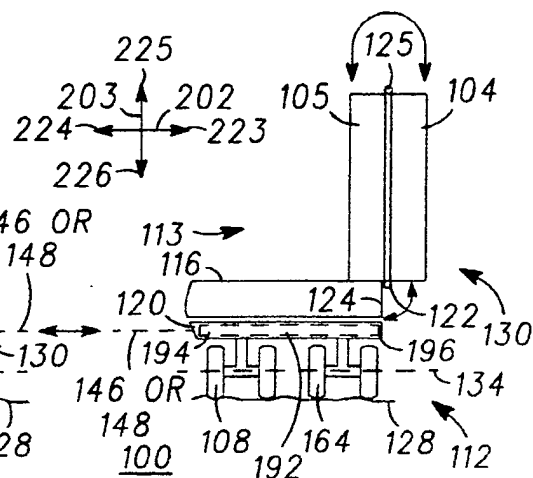


FIG. 31

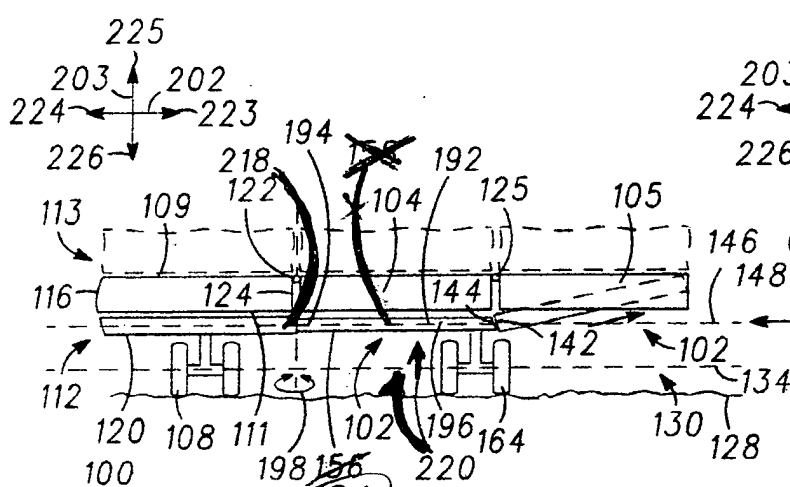


FIG. 32

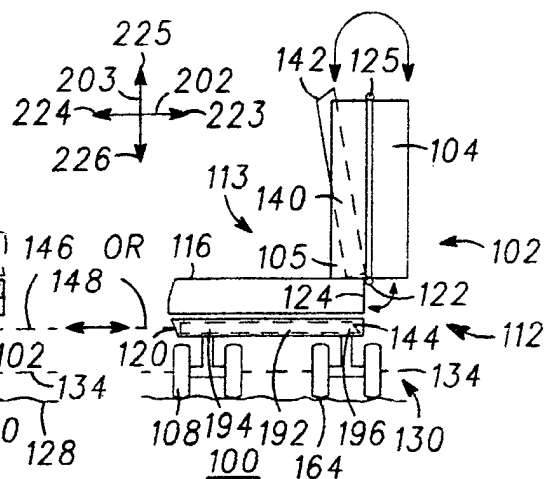


FIG. 33

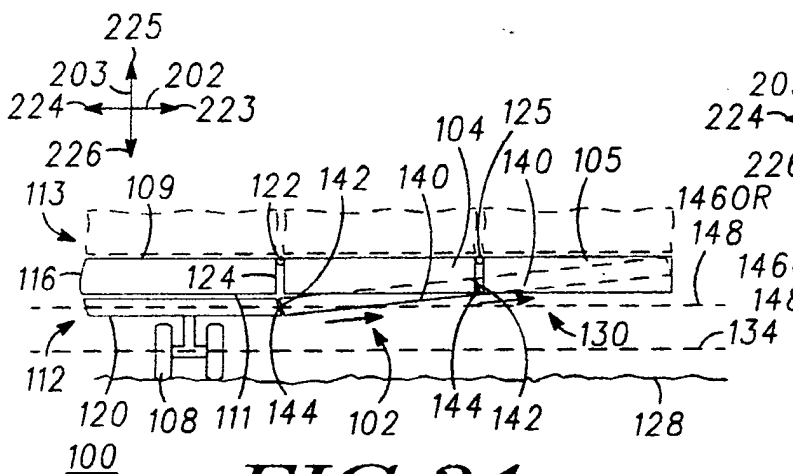


FIG. 34

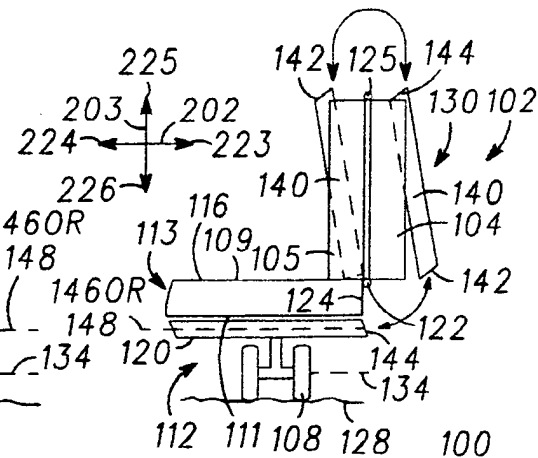


FIG. 35

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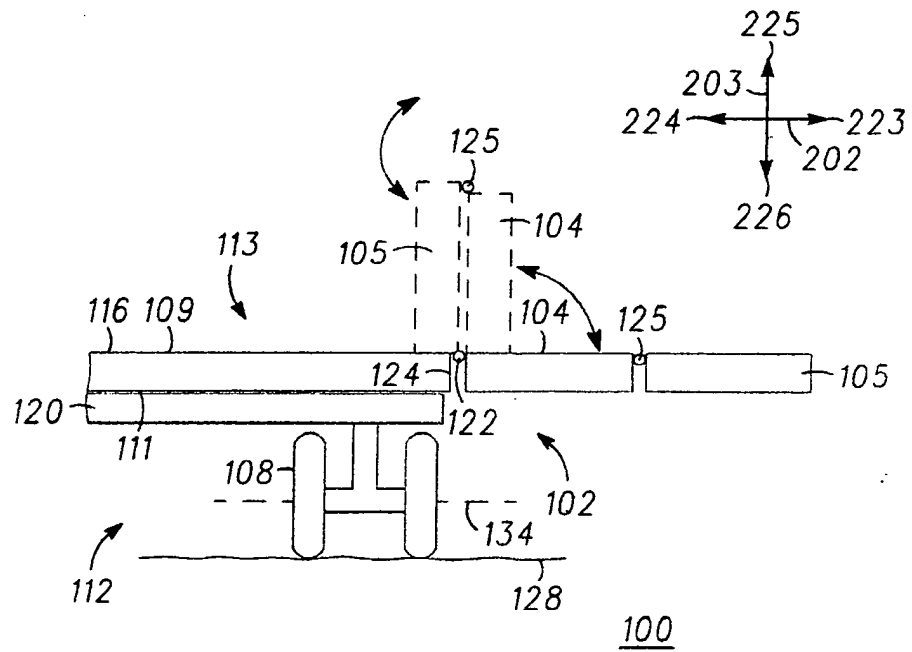


FIG. 38

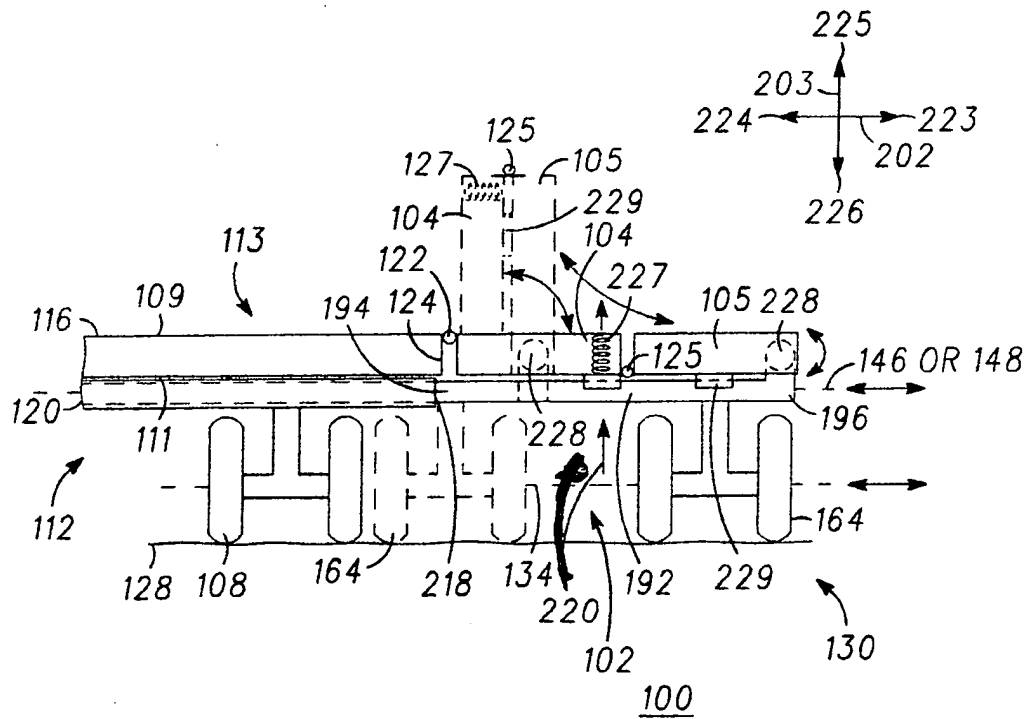


FIG. 39

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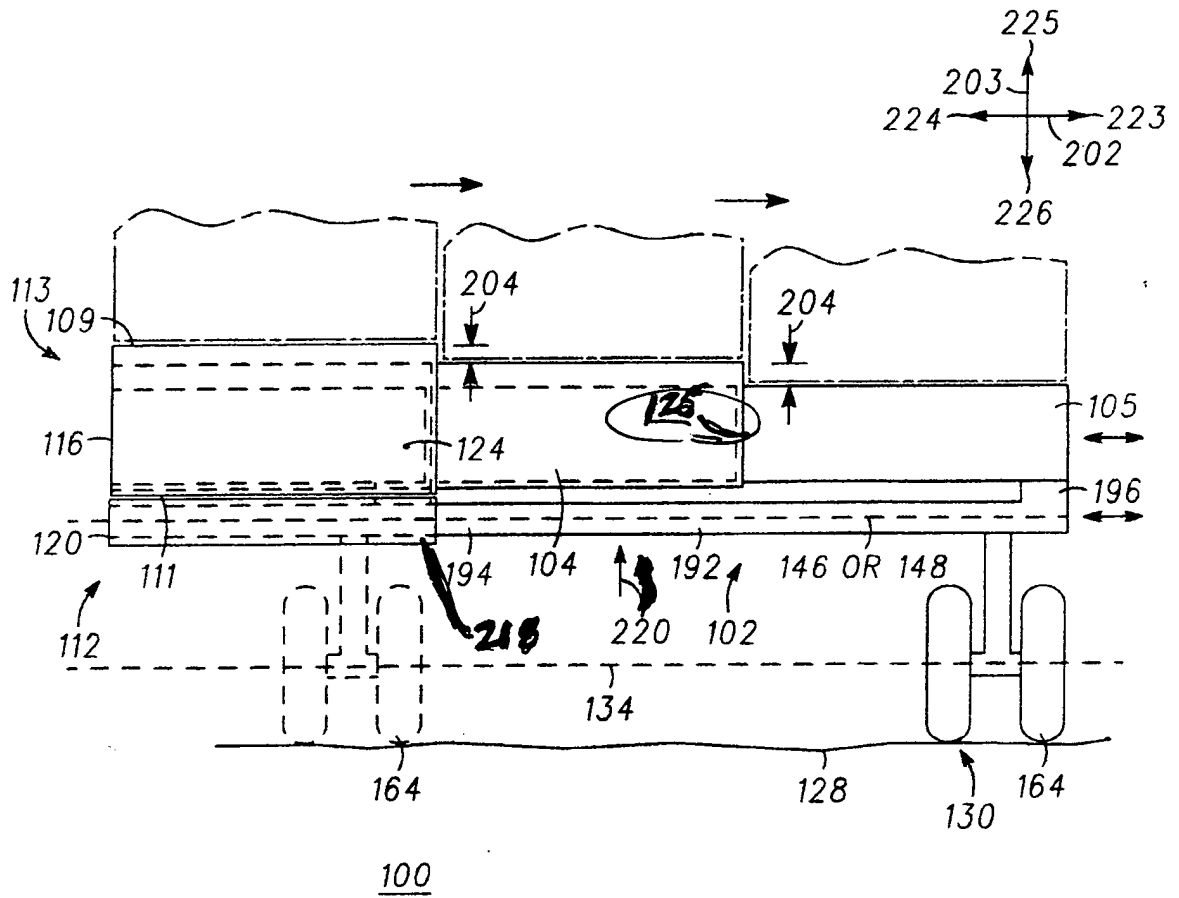


FIG. 40